CLAIMS

Having described the invention, what is claimed is:

1. A method of separating noise from a signal on a signal line to a digital circuit, comprising the steps of:

determining one or more edges of the noise relative to a fast clock;

resetting a timer according to the edges;

clocking output from the timer relative to a slow clock, the slow clock being slower than the fast clock; and

communicating a first value from the signal to the digital circuit after a period, defined by the slow clock, within which the timer has not reset.

2. The method of claim 1, wherein the step of resetting the timer comprises asynchronously resetting the timer.

3. The method of claim 1, wherein the step of determining the one or more edges comprises the steps of utilizing an edge detector having a first flip-flop and inputting the signal to an input of a first flip-flop.

4. The method of claim 3, further comprising the step of outputting a B signal value at an output of the first flip-flop.

5. The method of claim 4, wherein the step of outputting the B signal comprises latching the B signal value to a second value of the signal occurring at rising edges of the fast clock.

6. The method of claim 4, further comprising the step of digitally comparing the B signal value to the signal.

7. The method of claim 6, wherein the step of digitally comparing comprises the step of utilizing an XOR gate.

8. The method of claim 7, further comprising the step of communicating an output of the XOR gate to the timer.

9. The method of claim 1, wherein the step of communicating comprises the step of clocking a second flip-flop from an output of the timer.

10. The method of claim 9, further comprising the step of inputting the signal to the second flip-flop.

11. The method of claim 9, wherein the step of communicating comprises the step of outputting a value of the signal through the second flip flop and to the digital circuit, when clocked by the timer.

12. The method of claim 1, wherein the step of determining one or more edges of the noise relative to a fast clock comprises determining the one or more edges at a fast clock rate of at least about one megahertz

13. The method of claim 12, wherein the step of clocking output of the timer comprises clocking output of the timer at a clock rate that is at least about a factor of 1000 slower than the fast clock rate.

14. Logic apparatus for filtering noise from a signal on a signal line to a digital circuit, comprising:

an edge detector for detecting edges of the noise and relative to a fast clock; and

a timer for clocking a latch to a value of the signal line and relative to a slow clock, the slow clock being slower than the fast clock, the timer being reset by one or more signals from the edge detector and corresponding to the edges, the latch occurring after a time period defined by the slow clock within which the timer has not reset.

15. Apparatus of claim 14, the timer being asynchronously reset by the signals from the edge detector.

16. Apparatus of claim 15, further comprising a first flip flop connected to the timer and the signal line, the first flip flop latching the value of the signal when clocked by the timer.

17. Apparatus of claim 16, wherein the first flip flop comprises a D flip flop, the signal line being coupled a D input to the D flip flop.

18. Apparatus of claim 14, wherein the edge detector comprises a second flip flop and a digital comparator, the signal line being coupled to an input to the second flip flop, the second flip flop being clocked by the fast clock to produce a B signal value at an output of the second flip flop, the B signal corresponding to a value of the signal line at a rising edge of the fast clock, the digital comparator comparing the value of the signal to the B signal value for input to the timer.

19. Apparatus of claim 18, wherein the second flip-flop comprises a D flip-flop, and wherein the digital comparator comprises an XOR gate.